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EXAMINER	
CRUTCHFIELD, CHRISTOPHER M	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 10/589,922	Applicant(s) VAN DALEN ET AL.	
	Examiner Christopher Crutchfield	Art Unit 2466	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _25 August 2010_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-9_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-5,8 and 9_ is/are rejected.

7)☒ Claim(s) _6 and 7_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

   1. Determining the scope and contents of the prior art.
   2. Ascertaining the differences between the prior art and the claims at issue.
   3. Resolving the level of ordinary skill in the pertinent art.
   4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. **Claims 1, 2, 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Srikanteswara*, et al. (S. Srikanteswara, J. Reed, P. Athanas, R. Boyle, A Soft Radio Architecture for Reconfigurable Platforms, IEEE Communications Magazine, Feb. 2000, Pages 140-147) in view of *Marinissen I*, et al. (E. Marinissen I , Y. Zorian , R. Kapur , T. Taylor and L. Whetsel, Towards a Standard for Embedded Core Test: An Example, Proceedings of the IEEE International Test Conference, Pages 616-627, 1999) and *Marinissen II*, et al. (E. Marinissen, R. Kapur, M. Lousberg, T. McLaurin, M. Ricchetti and Y. Zorian, On IEEE P1500's Standard for Embedded Core Test, Journal of Electronic Testing, Springer Netherlands, Issue Volume 18, Numbers 4-5 / August, 2002, Pages 365-383).

Regarding claim 1, *Srikanteswara* discloses an electronic signal processing circuit, comprising:

a. A plurality of chained stream processing circuits, each having a stream input and a stream output, for inputting and outputting an input and output stream of successive sample values (Pages 142-147). (The system of *Srikanteswara* discloses a stream based processing architecture for software radios [Pages 142-143]. The architecture operates by programming individual processing elements [i.e. stream processing circuits] to perform discrete functions for the software radio [See Figs. 1 and 2, and Pages 143-144, "The Processing Layer]. The processing element I/O's are linked by a bus [i.e. the linking circuit] which feeds the stream of sampled data from, for example, the A/D converter [See Fig. 1, “Data from A/D Converter”] through the processing elements where the desired functions are performed on the data [See, for example,

Pages 144-147, “Implementation of an Adaptive Single User CDMA Receiver” - Showing the stream processing for a CDMA Receiver].)

b. Linking circuits, each linking a respective pair of stream processing circuits, each linking in a normal mode, the linking circuit, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits in the respective pair (Pages 142-147 - See (a), Supra).

Srikanteswara fails to disclose the use of test access points for each of the streamed processing circuits to allow for test access to the inputs and outputs of the stream processing circuits such that the system further comprises linking multiplexing circuits, each linking a respective pair of stream processing circuits, each linking multiplexing circuit being individually switchable to a normal mode and to a replacement mode, the linking multiplexing circuit, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits in the respective pair and the system further comprises a shareable communication structure coupled to the linking multiplexing circuits, each linking multiplexing circuit, when in the replacement mode, providing a continuous connection for supplying successive sample values from a second stream from the communication structure to a receiving one of the stream processing circuits in the respective pair of the stream processing circuits and a control circuit coupled to the linking multiplexing circuits, arranged to keep a selectable one of the multiplexing circuits in the replacement mode so that the selectable one of the linking multiplexing circuits passes a stream of successive sample from the second stream to the receiving one of the processing circuits in the respective

pair of linking multiplexing circuit, while keeping at least part of the other linking multiplexing circuits in the normal mode.

In the same field of endeavor, *Marinissen I* discloses the use of test access points for each of the streamed processing circuits to allow for test access to the inputs and outputs of the stream processing circuits such that the system further comprises:

a. Linking multiplexing circuits, each linking a respective pair of stream processing circuits, each linking multiplexing circuit being individually switchable to a normal mode and to a replacement mode, the linking multiplexing circuit, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits in the respective pair and a shareable communication structure coupled to the linking multiplexing circuits, each linking multiplexing circuit, when in the replacement mode, providing a continuous connection for supplying successive sample values from a second stream from the communication structure to a receiving one of the stream processing circuits in the respective pair of the stream processing circuits (Pages 616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing the multiple cores connected in parallel via their input and outputs]. The second input is connected to

the serial TestRail [i.e. communication structure] and is used for supplying test values to the inputs of the cores when the core is in the serial internal test mode [i.e. replacement mode] [See Fig. 8(d)].)

c. A control circuit coupled to the linking multiplexing circuits, arranged to keep a selectable one of the multiplexing circuits in the replacement mode so that the selectable one of the linking multiplexing circuits passes a stream of successive sample from the second stream to the receiving one of the processing circuits in the respective pair of stream processing circuits (Page 621, Fig. 3 and Pages 625-626, Figs 7, 8 and Table 3). (The system of *Marinissen I* discloses that the control circuit sets the mode of the linking multiplexing circuit via the WC connections [Page 621, Fig. 3], which control the connections of the wrapper input cell multiplexer to set the mode of the core [See Pages 625-626, Fig. 7(b), Figs 8(a) and (d) and Table 3]. When one of the link multiplexing circuit is set in the internal test mode, samples form the second stream/test rail are passed into the core/processor via the “wci” multiplexer [Pages 625-626, Fig. 7(b) and Table 3].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the

remainder of the chained processors/cores in bypass mode. The motive to combine is provided by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

Marinissen I fails to disclose that the control circuit keeps a selectable one of the multiplexing circuits in the replacement mode while keeping at least part of the other linking multiplexing circuits in the normal mode. In the same field of endeavor, *Marinissen II* discloses that the control circuit keeps a selectable one of the multiplexing circuits in the replacement mode while keeping at least part of the other linking multiplexing circuits in the normal mode (Pages 378-381, Figs. 11(a) and 11(b), Table 2 and the Last Paragraph of Page 378, carried onto Page 381). (The system of *Marinissen II* discloses the fact that the cores/stream processors in the normal and bypass modes have non-conflicting inputs to the multiplexers [i.e. as shown in table 2, the set bits in the normal mode correspond to the dont care bits in the bypass mode and vice versa]. Therefore, the system of *Marinissen II* collapses the Bypass and the Normal mode into a single mode [See The Last Paragraph of Page 378, carried onto Page 381]. The result of this operation is that when all of the cores except the core under test [which is placed into the replacement or serial internal test mode] are placed into the bypass mode [as suggested by both *Marinissen I* and *Marinissen II*] the cores are also in the normal functional mode. The same technique can also be applied to *Marinissen I* which has a similar arrangement of don’t care bits in the normal and serial bypass modes [See *Marinissen I*, Page 626, Table 3].)

Therefore, since *Marinissen II* suggests collapsing the bypass and normal operating modes into a single mode, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the collapsed modes of *Marinissen II* into the teachings of *Srikanteswara* as modified by *Marinissen I* by collapsing the control inputs for setting the normal

and bypass mode into a single set of inputs. The motive to combine is to reduce the instruction set size of the wrapper instruction register.

Regarding claim 2, *Srikanteswara* fails to disclose an electronic signal processing circuit comprising interface circuits, each coupled between the communication structure and the stream output of a respective one of the stream processing circuits, each interface circuits being individually switchable to an output mode under control of the control circuit (IS), each interface circuit, when in the output mode, passing successive samples of the second stream or a further stream from the stream output of a respective one of the stream processing circuits to the communication structure. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing circuit comprising interface circuits, each coupled between the communication structure and the stream output of a respective one of the stream processing circuits, each interface circuits being individually switchable to an output mode under control of the control circuit (IS), each interface circuit, when in the output mode, passing successive samples of the second stream or a further stream from the stream output of a respective one of the stream processing circuits to the communication structure (Pages 289, Fig. 5 and 292, Fig. 10(a)). (The system of *Marinissen I* further discloses that in addition to inserting samples at the input ports of the cores/stream processors via the linking multiplexer, the system may also capture the output of each of the cores/stream processors made in response to an input test stream [i.e. the “second stream”] inserted from the serial TestRail [i.e. communications structure] by using a multiplexer [i.e. interface circuit] [See Page 625, Fig. 7(c), The multiplexer controlled by the “wco” input] attached to the output of the core and may re-direct the core output to the system TestRail [i.e. communications structure] [See Pages 625-262, Fig. 8(d), Fig. 7(c) and Table 3].)

Therefore, since *Marinissen I* suggests the use of output re-direction of test streams for core testing, it would have been obvious to a person of ordinary skill in the art at the time of the

invention to combine the output re-direction of *Marinissen I* with the stream processors of *Srikanteswara* by using the TestRail/communications structure and the link multiplexing circuit to introduce a test/second stream to the input of a core/stream processor to be tested, and to then use the interface circuit/output multiplexer to capture the result of the test and re-direct the test output to the TestRail/communication structure. The motive to combine is to allow observance of the response of cores to a particular input, thereby allowing the testing and observation of internal cores.

Regarding claim 8, *Srikanteswara* fails to disclose an electronic signal processing circuit comprised on an integrated circuit chip. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing circuit comprised on an integrated circuit chip (Pages 616-617). Therefore, since *Marinissen I* suggests placing multiple core processors on a single integrated circuit, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the chained streamed processors and the electronic signal circuit of *Srikanteswara* on a single IC. The motive to combine is to reduce costs by using a single IC to perform all the required tasks.

Regarding claim 9, *Srikanteswara* discloses a plurality of stream processing circuits that are connected in a network which passes streams of sample values between pairs of the stream processing circuits (Pages 142-147). (The system of *Srikanteswara* discloses a stream based processing architecture for software radios [Pages 142-143]. The architecture operates by programming individual processing elements [i.e. stream processing circuits] to perform discrete functions for the software radio [See Figs. 1 and 2, and Pages 143-144, "The Processing Layer”]. The processing element I/O's are linked by a bus [i.e. the linking circuit] which feeds the stream of sampled data from, for example, the A/D converter [See Fig. 1, “Data from A/D Converter] through the processing elements where the desired functions are

performed on the data [See, for example, Pages 144-147, “Implementation of an Adaptive Single User CDMA Receiver” - Showing the stream processing for a CDMA Receiver].)

Srikanteswara fails to disclose a method further comprising an electronic signal processing circuit that comprises a plurality of stream processing circuits that are connected in a network which passes streams of sample values between pairs of the stream processing circuits, the method comprising providing a shareable communication structure coupled to stream inputs and outputs of the stream processing circuits, the shareable communication structure being redundant during normal use of the electronic signal processing circuit and in a test mode, extracting output streams from selected normally internal stream processing circuits or supplying input streams to selected normally internal stream processing circuits via the shareable communication structure. In the same field of endeavor, *Marinissen I* discloses a method further comprising an electronic signal processing circuit a that comprises a plurality of stream processing circuits that are connected in a network which passes streams of sample values between pairs of the stream processing circuits, the method comprising providing a shareable communication structure coupled to stream inputs and outputs of the stream processing circuits, the shareable communication structure being redundant during normal use of the electronic signal processing circuit and in a test mode, extracting output streams from selected normally internal stream processing circuits or supplying input streams to selected normally internal stream processing circuits via the shareable communication structure (Pages 616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the

output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing the multiple cores connected in parallel via their input and outputs]. The second input is connected to the serial TestRail [i.e. communication structure] and is used for supplying test values to the inputs of the cores when the core is in the serial internal test mode [i.e. replacement mode] [See Fig. 8(d)]. The serial test rail is redundant and is not used for communication between the cores when the system is operating in normal mode [See Fig. 8(a)].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. The motive to combine is provided by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

5. **Claims 3-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Srikanteswara*, et al. (S. Srikanteswara, J. Reed, P. Athanas, R. Boyle, A Soft Radio Architecture for Reconfigurable Platforms, IEEE Communications Magazine, Feb. 2000, Pages 140-147) in view of *Marinissen I*, et al. (E. Marinissen I , Y. Zorian , R. Kapur , T. Taylor and L.

Whetsel, Towards a Standard for Embedded Core Test: An Example, Proceedings of the IEEE International Test Conference, Pages 616-627, 1999) and *Marinissen II*, et al. (E. Marinissen, R. Kapur, M. Lousberg, T. McLaurin, M. Ricchetti and Y. Zorian, On IEEE P1500's Standard for Embedded Core Test, Journal of Electronic Testing, Springer Netherlands, Issue Volume 18, Numbers 4-5, August, 2002, Pages 365-383) as applied to claim 2 and further in view of *Zorian*, et al. (Y. Zorian, E. Marinissen I, S. Dey, Testing Embedded-Core Based System Chips, Proceedings of the IEEE International Test Conference, 1998, Pages 130-143).

Regarding claim 3, *Srikanteswara* fails to disclose an electronic signal processing circuit according wherein the communication structure comprises a plurality of chained multiplexing circuits, individually controllable by the control circuit, each chained multiplexing circuit corresponding to a respective corresponding one of the stream processing circuits, each having a first input, a second input and an output, the first input being coupled to the stream output of the corresponding one of the stream processing circuits, the second input being coupled to the output of the chained multiplexing circuit a preceding one of the stream processors. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing circuit according wherein the communication structure comprises a plurality of chained multiplexing circuits, individually controllable by the control circuit, each chained multiplexing circuit corresponding to a respective corresponding one of the stream processing circuits, each having a first input, a second input and an output, the first input being coupled to the stream output of the corresponding one of the stream processing circuits, the second input being coupled to the output of the chained multiplexing circuit of a preceding one of the stream processors (Figs. 7 and 8). (The system of *Marinissen I* discloses the use of a bypass circuit connected to a multiplexer [i.e. the chained multiplexing circuit] [See Fig. 7(a), “Bypass” and the

“m5” multiplexer]. The chained multiplexing circuit is connected to two inputs. The first is the connected to the output of the associated stream processing circuit [See Fig. 5(a), "M6" the upper connection to the outputs of core A][i.e. the stream output of the corresponding stream processing circuit]. The second is connected to the previous core/chain processor via the serial TestRail/shareable communication structure [See Fig. 7(a), "si", “bypass”, "m6” - Showing the lower connection to the chain multiplexer connected to the so output of the previous core], which is in turn connected to the output of the previous core's/processor’s chained multiplexing circuit [See Fig. 7(a), “so”].)

Therefore, since *Marinissen I* suggests the use of a chained multiplexer to allow a bypass mode for the serial TestRail, it would have been obvious to a person of ordinary skill in the art at the time of the invention to implement the bypass and chained multiplexer of *Marinissen I* into the teachings of *Srikanteswara* by inserting a bypass register and chained multiplexer into the shareable communications structure of *Srikanteswara* as modified by *Marinissen I*. The motive to combine is provided by is to reduce the time necessary to access each of the cores by allowing the bypassing of cores not involved in the present testing.

Srikanteswara as modified by *Marinissen I* fails to disclose an electronic signal processing circuit wherein the communication structure further comprises a plurality of chained multiplexing circuits wherein the second input is coupled to the output of the chained multiplexing circuit that corresponds to a preceding one of the stream processing circuit whose stream output is linked to the corresponding one of the stream processing circuit by one of the multiplexing circuits (i.e. *Marinissen I* fails to disclose that the connection order of the TestRail chains via the chained multiplexers coincides with the order of the input-output flow of data through the chained processors). In the same field of endeavor, *Zorian* discloses a plurality of chained multiplexing circuits wherein the second input is coupled to the output of the chained

multiplexing circuit that corresponds to a preceding one of the stream processing circuit whose stream output is linked to the corresponding one of the stream processing circuit by one of the multiplexing circuits (Figs. 5 and 6 and Pages 135-136, Section 6). (*Zorian* discloses a series of cores/processors which are linked up to form a chain in which the outputs of each core are connected to the inputs of the next core [See Fig. 6, Connections between Cores A, B and C]. *Zorian* further discloses that the test rail/communications structure connection via the chained multiplexing circuits may follow a path that coincides with the chained flow of the input-output ports of the processors [See Fig. 5, the TestRail connection that is connected through cores A, B and C].)

Therefore, since *Zorian* suggests the use of a TestRail flow via chained multiplexers that matches the direction flow of inputs and outputs through a series of chained processors, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the system of *Zorian* with the teachings of *Srikanteswara* as modified by *Marinissen I* by connecting the test rail and chained multiplexer connections in the same direction as the flow of data through the chained processors. The motive to combine is to make the ordering of the processors/cores on the TestRail connection easier to comprehend by ordering the TestRail connections in the same direction and order as the flow of data through the cores and to allow rapid testing of the interconnections between the processors (i.e. if the order of the flow of data over the TestRail did not match the order of the flow of data through the interconnections through the chained cores, it would not be possible to directly test all the interconnects between each of the cores using a serial test bus by continuously providing input data at the output of an upstream core associated with a link to be tested and continuously capturing the data on the other side of the connection at the input of the downstream core because the input test stream and the output result stream would “cross” on the serial TestRail for some subset of the directly

connected cores and would have to be multiplexed, reducing speed and requiring additional data capture circuitry.)

Regarding claim 4, *Srikanteswara* fails to disclose an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits (Pages 616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing the multiple cores connected in parallel via their input and outputs]. The second input is connected to the serial TestRail [i.e. communication structure] and is used for supplying test values to the inputs of the cores from the chained multiplexing circuit [See Fig. 7(b) - from chip]. The test values [i.e. samples of the second stream] are supplied from the core’s chained

multiplexing circuit, which receives the values via its second input from the previous core's chain multiplexing circuit [See Fig. 7, "m6", "si" and "so"] [See Also claim 3, Supra].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail containing the chained multiplexing circuits linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail using chained multiplexing circuits and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. The motive to combine is provided by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

Regarding claim 5, *Srikanteswara* fails to disclose an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits. In the same field of endeavor, *Marinissen I* discloses an electronic signal processing integrated circuit wherein each linking multiplexing circuit has a first input and a second input, the first input coupled to the stream output of a linked one of the stream processing circuits to receive sample values from the first stream, the second input receiving the second stream which is supplied to the second input of the chained multiplexing circuits that corresponds to the linked one of the stream processing circuits (Pages

616-617 and 618-625). (The system of *Marinissen I* discloses a system for testing cores [i.e. stream processing circuits] internal to an integrated circuit [Pages 616-617]. The system uses a multiplexer [i.e. the link multiplexing circuit] [See Fig. 7 (b), The mux with the wci input] with two inputs to select a signal to be input into a core in accordance with the operating mode of the particular core [See Pages 620-621 and Page 625, Fig. 8]. The first input is connected to the output of the previous core [i.e. the first stream form the upstream stream processing circuit] and is active when the device is in the “normal” mode [See Fig. 8 (a)] [See also Fig. 3 - Showing the multiple cores connected in parallel via their input and outputs]. The second input is connected to the serial TestRail [i.e. communication structure] and is used for supplying test values to the inputs of the cores from the chained multiplexing circuit [See Fig. 7(b) - from chip]. The test values [i.e. samples of the second stream] are supplied from the core’s chained multiplexing circuit, which receives the values via its second input from the previous core’s chain multiplexing circuit [See Fig. 7, “m6”, “si” and “so”] [See Also claim 3, Supra].)

Therefore, since *Marinissen I* discloses the use of a multiplexer for inserting and extracting test data from the inputs and outputs of the internal cores of an integrated circuit via a serial test rail containing the chained multiplexing circuits linking the individual cores, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of *Marinissen I* with the system of *Srikanteswara* by linking the individual chained processors/cores of *Srikanteswara* with a serial test rail using chained multiplexing circuits and providing a multiplexing circuit for inserting and extracting test data from the inputs and outputs of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. The motive to combine is provided by *Marinissen I* and is to allow direct access to the inputs and outputs of the individual cores/processors for testing (See *Marinissen I*, Pages 616-617, Introduction).

Srikanteswara as modified by *Marinissen I* fails to disclose an electronic signal processing circuit wherein each linking multiplexing circuit further comprises a second input receiving the second stream which is supplied to the second input of the chained multiplexing circuit that corresponds to the preceding one of the stream processing circuits whose stream output is linked to the input of the linked one of the stream processing circuits (i.e. *Marinissen I* fails to disclose that the connection order of the TestRail chains via the chained multiplexers coincides with the order of the input-output flow of data through the chained processors). In the same field of endeavor, *Zorian* discloses a plurality of chained multiplexing circuits wherein the second input is coupled to the output of the chained multiplexing circuit that corresponds to a preceding one of the stream processing circuit whose stream output is linked to the corresponding one of the stream processing circuit by one of the multiplexing circuits (Figs. 5 and 6 and Pages 135-136, Section 6). (*Zorian* discloses a series of cores/processors which are linked up to form a chain in which the inputs of each core are connected to the outputs of the next core [See Fig. 6, Connections between Cores A, B and C]. *Zorian* further discloses that the test rail/communications structure connection via the chained multiplexing circuits may follow a path that coincides with the chained flow of the input-output ports of the processors [See Fig. 5, the TestRail connection that is connected through cores A, B and C].)

Therefore, since *Zorian* suggests the use of a TestRail flow via chained multiplexers that matches the direction flow of inputs and outputs through a series of chained processors, it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the system of *Zorian* with the teachings of *Srikanteswara* as modified by *Marinissen I* by connecting the test rail and chained multiplexer connections in the same direction as the flow of data through the chained processors. The motive to combine is to make the ordering of the processors/cores on the TestRail connection easier to comprehend by ordering the TestRail

connections in the same direction and order as the flow of data through the cores and to allow rapid testing of the interconnections between the processors (i.e. if the order of the flow of data over the TestRail did not match the order of the flow of data through the interconnections through the chained cores, it would not be possible to directly test all the interconnects between each of the cores using a serial test bus by continuously providing input data at the output of an upstream core associated with a link to be tested and continuously capturing the data on the other side of the connection at the input of the downstream core because the input test stream and the output result stream would “cross” on the serial TestRail for some subset of the directly connected cores and would have to be multiplexed, reducing speed and requiring additional data capture circuitry.)

Response to Arguments

6. Applicant's arguments filed 25 August 2010 have been fully considered but they are not persuasive.

Regarding claims 1-5, 8 and 9, Applicant’s Arguments that the office action is “not based on a rational underpinning” as it fails to "supply articulate reasoning" as to the conclusion of obviousness, Applicant's arguments have been considered and are not persuasive. The applicant is referred to the rejection of claims 1-5, 8 and 9, supra, which gives specific reasons under the teaching-suggestion-motivation test to support the findings of obviousness.

Regarding claims 1-5, 8 and 9, Applicant’s Arguments that the combination of *Srikanteswara* with *Marinissen* I and *Marinissen* II, is improper because the combination would

change the principal of operation of the system of *Srikanteswara*, Applicant's argument have been considered and are not persuasive.

The Applicant argues that the combination of *Srikanteswara* with *Marinissen* I and *Marinissen* II, is improper because the combination would change the principal of operation of the system of *Srikanteswara*, as the insertion and removal of test data into one of the stream processors would interfere with the flow of the stream data from one of the stream processors to another as "the configuration and the data processing of each of the processing modules in the processing layer of *Srikanteswara* would be interrupted by the newly added test data through the multiplexing circuit of *Marinissen* I." (Pages 9-10 of Applicant's arguments and Remarks, Filed 25 August 2010). Although this statement is true, it is unclear how this fundamentally alters the principal of operation of the system of *Srikanteswara*, as it merely introduces a method for providing individual test access to each of the cores and still allows for the normal operation of the system in non-test mode. Furthermore, even if one were to presume that the fundamental operation of *Srikanteswara* was modified by its combination with *Marinissen* I and *Marinissen* II, to the extent that the rejection is consistent with the "common sense" approach to obviousness presented in KSR Int'l Co. v. Teleflex Inc ("KSR") the holding of In re Ratti cannot be maintained. KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, USPQ2d 1385 (2007).

In order to fundamentally alter the principal of operation of a system, the modification must be such that "… [The] suggested combination of references would require a substantial reconstruction and redesign of the elements…as well as a change in the basic principles under which the…construction was designed to operate." In re Ratti, 270 F.2d 810, 813, 123 USPQ 349, 353 (CCPA 1959). For example, in In re Ratti, the court found that the replacement of a metal casing used to reinforce a rubber "press fit" ring for sealing the gap between a shaft (i.e. a piston) and a bore (i.e. cylinder) with a set of springs used to force the seal against the cylinder

walls changed the fundamental operation of the device because it replaced a mechanism which sealed the gap by "press fitting" the seal and the reinforcement with one that sealed the gap by means of the radially biased springs which served to press the seal against the walls of the cylinder. *Id* at 350-352. This modification was important because it allowed the seal to be maintained, even after the "resiliency" of the rubber ring was lost, as the radial force of the springs would maintain contact between the seal and the cylinder wall. *Id* at 351-52. Therefore, under In re Ratti in order to "change a basic principle" under which the construction was designed to operate, the change must be such as to alter a fundamental mechanism of action in the operation of the device[1].

Furthermore, The Standard of In re Ratti must also now be interpreted in light of The Courts findings in KSR Int'l Co. v. Teleflex Inc. ("KSR"). KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, USPQ2d 1385 (2007). In KSR, The Court eschewed an overly rigid approach to the patentability determination, noting that:

> "…if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond that person's skill." *Id* at 1389.

> "…common sense teaches…that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle…" *Id* at 1390.

[1] It is also noteworthy that in the decision in In re Ratti, the court also appeared to rely heavily on other factors in making the decision, such as the fact that the field of the endeavor of the secondary reference (Sealing a coffee maker) was only tangentially related to the field of endeavor of the Applicant's invention (Oil seals in aircraft engines) and the presence of a bias due to hindsight reconstruction. In re Ratti at 351-354.

It is unclear to what extent, if at all, In re Ratti is in opposition to KSR v. Teleflex. Nevertheless, what is clear is that any interpretation of In re Ratti that is inconsistent with the "common sense" approach of KSR to obviousness is no longer valid[2].

Turning to the claims at hand, The Applicant argues that the principal of operation of the system of *Srikanteswarai* would be fundamentally altered by its combination with the system of *Marinissen* I and *Marinissen* II because the system of *Srikanteswarai* would no longer sequentially perform operations on a stream of data that flows between the various processing modules, as the stream would be "broken" in order to insert and extract the test data. In effect, the applicant asserts that the principal of operation of the system of *Srikanteswarai* is the streaming of data between the various processing modules and that that this principal is fundamentally altered by its combination with *Marinissen* I and *Marinissen* II. The Examiner agrees that it appears that one of the principals of operation of the system of *Srikanteswarai* is the use of stream processing. However, the combination of *Srikanteswarai* with *Marinissen* I and *Marinissen* II does not alter this principal, but rather improves it, as the system of *Srikanteswarai* still uses stream processing for regular operations, but now includes an additional mode that allows specific test data to be introduced to and extracted from the stream processors.

Furthermore, even if Applicant's Arguments that the principal of operation of *Srikanteswarai* would be altered by its combination with systems of *Marinissen* I and *Marinissen* II were to be accepted, the finding under In re Ratti would have to be abrogated to the extent it

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[2] See For Example, Ex Part Robert (BPAI Non-Precedential Opinion, Appeal No. 2009-005757, 27 April 2010). ("Appellant's argument is based on a reading of In re Ratti, 270 F.2d 810 (CCPA 1959). We have reviewed that venerable case of the CCPA, and find that much of its holding must be updated by further developments in the law guided by the Supreme Court as expressed in KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398 (2007). Rather than express obviousness as the physical placement of structure (i.e., an oil seal made of resilient deformable material) from one reference within the confines of the structure (i.e., a cylindrical bore surrounding a relatively movable shaft) from another reference, in KSR the Supreme Court viewed the prior art as a combination of teachings from different sources, and the use of those teachings by a practitioner in the art.")

is inconsistent with a rejection of claims 1-5, 8 and 9 under KSR. For example, instead of viewing the combination of *Srikanteswarai* with *Marinissen* I under a traditional teaching-suggestion-motivation test, as presented in claim 1, one could instead view *Srikanteswarai* as teaching a base device that includes a plurality of stream processing circuits that may be embodied as individual processors (i.e. embedded cores) (See Pages 145-146 - The Stallion Architecture) and a linking circuit and the system of *Marinissen* I as teaching a known technique for improving access to embedded cores, comprising allowing the introduction and extraction of test data from each of the cores by means of a multiplexed test rail (i.e. sharable communications structure). KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, USPQ2d 1385, 1389-1390. Therefore, the claimed invention would have been obvious, as a person of ordinary skill in the art at the time of the invention could have applied the embedded core access technique of *Marinissen* I to the streaming processors of *Srikanteswarai* (which are likewise individual cores embedded in a single silicon device) to produce the predictable result of allowing individualized test access to each of the streaming processors. Based on the presented rationale under KSR, it is clear that the combination of *Srikanteswarai* with *Marinissen* I is proper and therefore to the extent that In re Ratti is inconsistent with this finding, it is overruled.

Allowable Subject Matter

7. **Claims 6 and 7** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Crutchfield whose telephone number is (571) 270-3989. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daniel Ryman can be reached on (571) 272-3152. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher Crutchfield/
Examiner, Art Unit 2466
10/25/2010

/Daniel J. Ryman/
Supervisory Patent Examiner, Art Unit 2466